Customer No.: 31561
Docket No.: 13129-US-PA
Application No.: 10/711,835

## REMARKS

### Present Status of the Application

The Office Action rejected claims 1-2, 5-6, 13-14, 17-18 under 35 U.S.C. 102(b), as being anticipated by Takahata et al. (JP 05-257167). The Office Action also rejected claims 3-4, 7-12, 15-16 under 35 U.S.C. 103(a) as being unpatentable over Takahata et al. (JP 05-257167) in view of Lee et al. (US 2006/0163582).

Applicant has amended claims 1, 4, 7, 10, 13 and 16 and canceled claims 2-3, 8-9 and 14-15 to more clearly define the present invention. After entry of the foregoing amendments, claims 1, 4-7, 10-13 and 16-18 remain pending in the present application, and reconsideration of those claims is respectfully requested.

### Discussion of Rejections

The Office Action rejected claims 1-2, 5-6, 13-14, 17-18 under 35 U.S.C. 102(b), as being anticipated by Takahata et al. (JP 05-257167). The Office Action also rejected claims 3-4, 7-12, 15-16 under 35 U.S.C. 103(a) as being unpatentable over Takahata et al. (JP 05-257167) in view of Lee et al. (US 2006/0163582).

Applicant has added the limitation of claim 3 into claim 1, added the limitation of claim 9 into claim 7 and added the limitation of claim 15 into claim 13. Applicant respectfully traverses the rejections for at least the reasons set forth below.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

"See M.P.E.P. 2143, Latest Revision August 2006".

The present invention is in general related a method of fabricating a gate, a method of fabricating a pixel unit and a method of fabricating a thin film transistor respectively as claims 1, 7 and 13 recite:

1. A method of fabricating a gate, comprising the steps of:

providing a substrate;

forming a patterned mask layer over the substrate, wherein the patterned mask layer exposes an area on the substrate for forming the gate;

forming a metallic layer over the mask layer and inside the exposed area such that the metallic layer formed over the mask layer is apart from the metallic layer formed inside the exposed area;

*forming an oxidation-resistant layer on the metallic layer, wherein the oxidation-resistant layer formed over the mask layer is apart from the oxidation-resistant layer formed inside the exposed area*; and

removing the mask layer, *wherein the metallic layer and the oxidation-resistant layer formed over the mask layer are removed at the same time and the metallic layer and the oxidation-resistant layer formed inside the exposed area is remained so as to form the gate.*

7. A method of fabricating a pixel unit, comprising the steps of:

providing a substrate;

forming a patterned mask layer over the substrate, wherein the patterned mask layer exposes an area on the substrate for forming the gate;

forming a metallic layer over the mask layer and inside the exposed area such that the metallic layer formed over the mask layer is apart from the metallic layer formed inside the exposed area;

***forming an oxidation-resistant layer on the metallic layer, wherein the oxidation-resistant layer formed over the mask layer is apart from the oxidation-resistant layer formed inside the exposed area;***

removing the mask layer, ***wherein the metallic layer and the oxidation-resistant layer formed over the mask layer are removed at the same time and the metallic layer and the oxidation-resistant layer formed inside the exposed area is remained so as to form the gate;***

forming an insulating layer over the substrate to cover the gate;

forming a channel layer over the insulating layer above the gate;

forming a source and a drain over the channel layer;

forming a passivation layer over the substrate, wherein the passivation layer has an opening that exposes a portion of the drain; and

forming a pixel electrode over the passivation layer such that the pixel electrode is electrically connected to the drain via the opening.

13. A method of fabricating a thin film transistor, comprising the steps of:

providing a substrate;

forming a patterned mask layer over the substrate, wherein the mask layer exposes an area on the substrate for forming the gate;

forming a metallic layer over the mask layer and inside the exposed area such that the metallic layer formed over the mask layer is apart from the metallic layer formed inside the exposed area;

***forming an oxidation-resistant layer on the metallic layer, wherein the oxidation-resistant layer formed over the mask layer is apart from the oxidation-resistant layer formed inside the exposed area;***

removing the mask layer, wherein ***the metallic layer and the oxidation-resistant layer formed over the mask layer are removed at the same time and the metallic layer and the oxidation-resistant layer formed inside the exposed area is remained so as to form the gate;***

forming an insulating layer over the substrate to cover the gate;

forming a channel layer over the insulating layer above the gate; and

forming a source and a drain over the channel layer.

The office action states Takahata does not teach the step of forming an oxidation-resistance layer, but Lee teaches the step of forming oxidation-resistance layer at paragraphs [0047]-[0048], [0070] and Figs. 5a-5b. However, applicant respectfully submits Lee does not teach the step of forming oxidation-resistance layer as claims 1, 7 and 13 recite. As a matter of fact, Lee teaches the gate wiring 22, 24, 26 is a two-layer structure formed of a first gate wiring layer 221, 241, 261 and a second gate wiring layer 222, 242, 262. The first gate wiring layer 221, 241, 261 is formed to improve adhesion to the substrate 10, and the second wiring layer 222, 242,

262 functions as a path for electric signal and is made of copper or copper alloy (see paragraph [0070]). In addition, Lee just teaches the copper alloy is used for the metal wiring material at paragraphs [0047]-[0048]. Therefore, applicant respectfully submits Lee fails to teach the step of ***forming an oxidation-resistance layer on the metallic layer*** because Lee does not teach the copper or copper alloy can function as an oxidation-resistance layer. Generally, copper or copper alloy is easily oxidized, and thus it cannot be used as an ***oxidation-resistance layer.*** Therefore, the copper or copper alloy of the Lee refcrence is different from the oxidation-resistance layer of the present invention in function, manner and result.

In addition, Lee teaches the gate line 22, 24, 26 (composed of the first gate wiring layer 221, 241, 261 and the second gate wiring layer 222, 242, 262) is formed with a photo-etched method (see paragraph [0082]). Therefore, Lee fails to teach the feature of the metallic layer and the oxidation-resistance layer are formed by the same lift-off process. That is, Lee does not teach the limitation of "forming an oxidation-resistant layer on the metallic layer, ***wherein the oxidation-resistant layer formed over the mask layer is apart from the oxidation-resistant layer formed inside the exposed area***" and "removing the mask layer, ***wherein the metallic layer and the oxidation-resistant layer formed over the mask layer are removed at the same time and the metallic layer and the oxidation-resistant layer formed inside the exposed area is remained so as to form the gate***" as claims 1, 7 and 13 recite.

Takahata just teaches the electrode Al is formed with a lift-off method. Takahata also fails to teach the feature of a metallic layer and an oxidation-resistance layer are formed by the

same lift-off process for forming a gate. Therefore, applicant respectfully submits the prior art references combined do not teach or suggest all the limitations in claims 1, 7, 13.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 7 and 13 patently define over the prior art references, and should be allowed. For at least the same reasons, dependent claims 4-6, 10-12 and 16-18 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim.

Customer No.: 31561
Docket No.: 13129-US-PA
Application No.: 10/711,835

## CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date : Dec 29, 2006

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw